Highly Integrated Protection System

The HIPS Platform: Forged on the Leading Edge of Advanced Reactor Ingenuity

HIPS
HIGHLY INTEGRATED PROTECTION SYSTEM

We hear you.

Today's nuclear power plant operators want safety-related systems that work for multiple decades without major upgrades. Previous generation digital I&C systems required frequent firmware updates and proved difficult to manage under current cybersecurity and regulatory constraints.

The SER-approved HIPS FPGA was designed with you in mind.

It doesn't attempt to push the boundaries of modern technology. It won't do your taxes, but it also won't raise eyebrows from upper management nor the NRC. It simply performs with robust, analog-like reliability while providing essential diagnostics for plants to reduce O&M costs.

Why is field programmable gate array (FPGA) technology the right choice for your nuclear power plant?

SIMILAR TO DIGITAL	... BUT BETTER
High reliability from comprehensive diagnostics & self-testing	✓ Deterministic—**costs less** to qualify
Flexible components (reconfigurable, reusable, portable logic)	✓ **Reduced complexity** means greater regulatory certainty
Fault tolerant	✓ **No executable software**
Software enhanced application development	✓ **Inherently more cyber-secure**
Configurable communications	✓ **Resilient to component obsolescence**
	✓ **Isolation of independent functions** (safety/non-safety) within the same system
	✓ **Quicker processing time** due to parallel execution of independent functions
	✓ Intuitive bypass and testability

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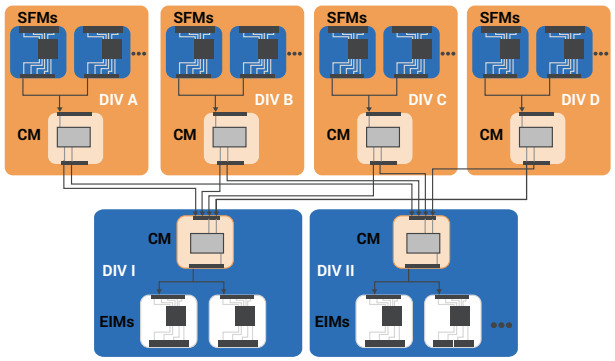
RPS Architecture

The scalable HIPS platform has complete architecture flexibility. It can be configured as a single channel or up to a full Reactor Protection System of four separation groups which votes into two divisions complete with physical and electrical isolation.



Model-Based Design

Model-Based Design provides a significant increase in the quality of the final product and reduction of project execution costs.

It's an all-in-one environment to meet the rigorous development requirements for safety critical systems in a significantly reduced development time by integrating both the system's functional behavior and the detailed description in one project model.

HIPS Model-Based Design automates error prone and time-consuming tasks, reducing the development time associated with code and document generation, test execution, and model checks.

Additionally, simulation of the system behavior provides the ability to examine its interaction with individual components to detect errors in requirements and design early in the development lifecycle before testing on expensive hardware.

Class-1E SER Approval

The HIPS platform topical report TR-1015-18653-P, Revision 0, "Design of the Highly Integrated Protection System [HIPS] Platform" was submitted in 2015 in partnership with NuScale. Rev. 1 was submitted in 2016 with NRC SER approval granted in 2017.

Software CCF Mitigated by Internal Diversity

The diversity in our FPGA equipment, circuit designs, and software tools are the fundamental methods for mitigating the potential for digital Common Cause Failures (CCF) in the HIPS platform.

The platform design uses two diverse FPGA technologies to achieve equipment diversity: one is a one-time programmable (OTP) or flash-based FPGA, with the other a static random-access memory (SRAM) based FPGA.

The overall HIPS diversity approach aligns with NRC BTP 7-19 and provides additional benefits by simplifying the holistic I&C facility design, since a separate diverse actuation system is not required to mitigate digital CCFs.

The diversity approach also provides analytical and regulatory review benefits, since additional 'best estimate' consequence analysis is not required. This ensures a more efficient regulatory turnaround and quicker system build for a higher level of confidence in meeting your project deadlines.

Additional Specs

- Triple modular redundant (TMR) data processing, regardless of system scale
- Redundant, auctioneered power source
- Hot-swappable modules without interruption
- Secure functional independence by implementing each safety function on a different Safety Function Module, unlike a microprocessor-based system where the loss of the main processor defeats all function
- More resilient to component obsolescence due to portability of HDL to new hardware
- 19-inch cabinet mountable card frame, 10.5 inches tall by 15.75 inches deep

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